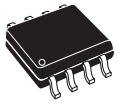
L5973D

2.5A SWITCH STEP DOWN SWITCHING REGULATOR

- 2.5A INTERNAL SWITCH
- OPERATING INPUT VOLTAGE FROM 4.4V TO 36V
- 3.3V / (±2%) REFERENCE VOLTAGE
- OUTPUT VOLTAGE ADJUSTABLE FROM 1.235V TO 35V
- LOW DROPOUT OPERATION: 100% DUTY CYCLE
- 250KHz INTERNALLY FIXED FREQUENCY
- VOLTAGE FEEDFORWARD
- ZERO LOAD CURRENT OPERATION
- INTERNAL CURRENT LIMITING
- INHIBIT FOR ZERO CURRENT CONSUMPTION
- SYNCHRONIZATION
- PROTECTION AGAINST FEEDBACK DISCONNECTION
- THERMAL SHUTDOWN



HSOP8 - EXPOSED PAD
ORDERING NUMBERS: L5973D (Tube)
L5973D013TR (T & R)

APPLICATIONS:

- CONSUMER: STB, DVD, TV, VCR,CAR RADIO, LCD MONITORS
- NETWORKING: XDSL, MODEMS,DC-DC MODULES
- COMPUTER: PRINTERS, AUDIO/GRAPHIC CARDS, OPTICAL STORAGE, HARD DISK DRIVE
- INDUSTRIAL: CHARGERS, CAR BATTERY DC-DC CONVERTERS

DESCRIPTION

The L5973D is a step down monolithic power switching regulator with a minimum switch current limit of 2.5A so it is able to deliver more than 2A DC current to the load depending on the application conditions.

The output voltage can be set from 1.235V to 35V.

The high current level is also achieved thanks to an SO8 package with exposed frame, that allows to reduce the $R_{th(j\text{-}amb)}$ down to approximately 40°C/W

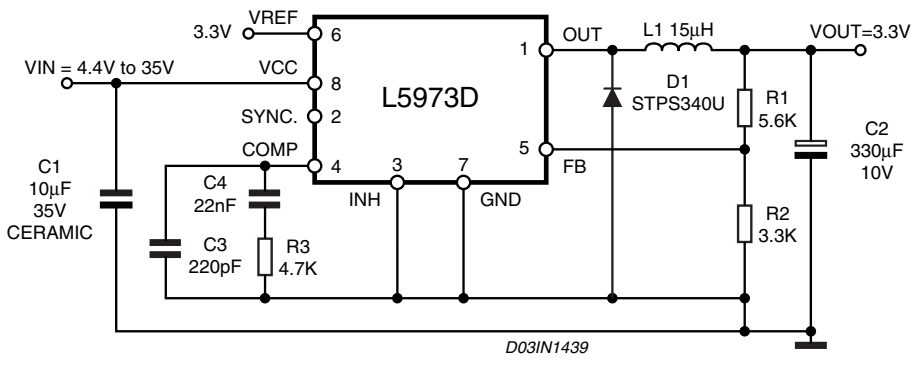
The device uses an internal P-Channel D-MOS transistor (with a typical Rdson of 250mΩ) as switching element to minimize the size of the external components.

An internal oscillator fixes the switching frequency at 250KHz.

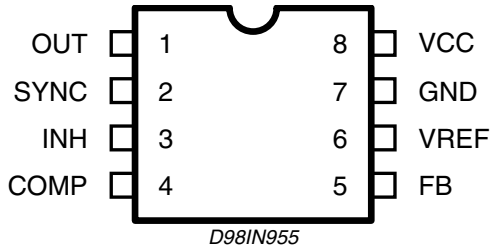
Having a minimum input voltage of 4.4V only, it is particularly suitable for 5V bus, available in all computer related applications.

Pulse by pulse current limit with the internal frequency modulation offers an effective constant current short circuit protection.

TEST APPLICATION CIRCUIT



PIN CONNECTION



D98IN955

PIN DESCRIPTION

N°	Pin	Function
1	OUT	Regulator Output.
2	SYNC	Master/slave synchronization.
3	INH	A logical signal (active high) disables the device. If INH not used the pin must be grounded. When it is open an internal pull-up disable the device.
4	COMP	E/A output for frequency compensation.
5	FB	Feedback input. Connecting directly to this pin results in an output voltage of 1.23V. An external resistive divider is required for higher output voltages.
6	VREF	3.3V V_{REF}. No cap is requested for stability.
7	GND	Ground.
8	VCC	Unregulated DC input voltage.

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j\text{-}amb)}$	Thermal Resistance Junction to ambient	Max.	40 (*)	°C/W

(*) Package mounted on board

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_8	Input Voltage	40	V
V_1	Output DC voltage Output peak voltage at t = 0.1µs	-1 to 40 -5 to 40	V V
I_1	Maximum output current	int. limit.	
V_4, V_5	Analog pins	4	V
V_3	INH	-0.3V to V_{CC}	
V_2	SYNC	-0.3 to 4	V
P_{tot}	Power dissipation at $T_{amb} \leq 60°C$	2.25	W
T_j	Operating junction temperature range	-40 to 150	°C
T_{stg}	Storage temperature range	-55 to 150	°C

ELECTRICAL CHARACTERISTICS (T_j = 25°C, V_{CC} = 12V, unless otherwise specified.)
(*) Specification Referred to Tj from -40 to 125°C (1).

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
V_{CC}	Operating input voltage range	V_o = 1.235V; I_o = 2A	*	4.4		36	V
R_{DSON}	Mosfet on Resistance		*		0.250	0.5	Ω
I_l	Maximum limiting current	V_{CC} = 4.4V to 36V		2.5	3	3.5	A
f_s	Switching frequency		*	212	250	280	KHz
				225	250	275	KHz
	Duty cycle			0		100	%
DYNAMIC CHARACTERISTICS (see test circuit).							
V_5	Voltage feedback	4.4V < V_{CC} < 36V, 20mA < I_O < 2A		1.220	1.235	1.25	V
			*	1.198	1.235	1.272	V
η	Efficiency	V_O = 5V, V_{CC} = 12V			90		%
DC CHARACTERISTICS							
I_{qop}	Total Operating Quiescent Current		*		3	5	mA
I_q	Quiescent current	Duty Cycle = 0; V_{FB} = 1.5V				2.5	mA
I_{qst-by}	Total stand-by quiescent current	V_{inh} > 2.2V	*		50	100	µA
		V_{CC} = 36V; V_{inh} > 2.2V	*		80	150	µA
INHIBIT							
	INH Threshold Voltage	Device ON				0.8	V
		Device OFF		2.2			V
ERROR AMPLIFIER							
V_{OH}	High level output voltage	VFB = 1V		3.5			V
V_{OL}	Low level output voltage	VFB = 1.5V				0.4	V
$I_{o\ source}$	Source output current	V_{COMP} = 1.9V; V_{FB} = 1V		200	300		µA
$I_{o\ sink}$	Sink output current	V_{COMP} = 1.9V; V_{FB} = 1.5V		1	1.5		mA
I_b	Source bias current				2.5	4	µA
	DC open loop gain	R_L = ∞		50	57		dB
gm	Transconductance	I_{comp} = -0.1mA to 0.1mA V_{COMP} = 1.9V			2.3		mS
SYNC FUNCTION							
	High Input Voltage	V_{CC} = 4.4V to 36V		2.5		V_{REF}	V
	Low Input Voltage	V_{CC} = 4.4V to 36V				0.74	V
	Slave Sink Current	V_{sync} = 0.74V (2) V_{sync} = 2.33V		0.11 0.21		0.25 0.45	mA mA
	Master Output Amplitude	I_{source} = 3mA		2.75	3		V
	Output Pulse Width	no load, V_{sync} = 1.65V		0.20	0.35		µs
REFERENCE SECTION							
	Reference Voltage			3.234	3.3	3.366	V
		I_{REF} = 0 to 5mA V_{CC} = 4.4V to 36V	*	3.2	3.3	3.399	V
	Line Regulation	I_{REF} = 0mA V_{CC} = 4.4V to 36V			5	10	mV
	Load Regulation	I_{REF} = 0 to 5mA			8	15	mV
	Short Circuit Current			10	18	30	mA

Notes: 1. Specification over the -40 to +125 Tj Temperature range are assured by design, characterization and statistical correlation.
2. Guaranteed by design.

Figure 1. Line Regulation

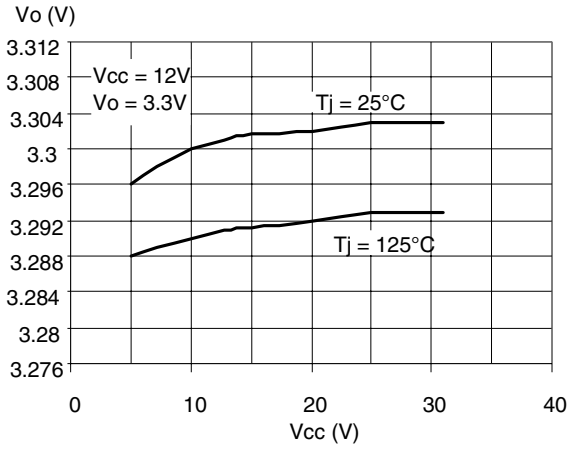


Figure 2. Output Voltage vs. Junction Temperature

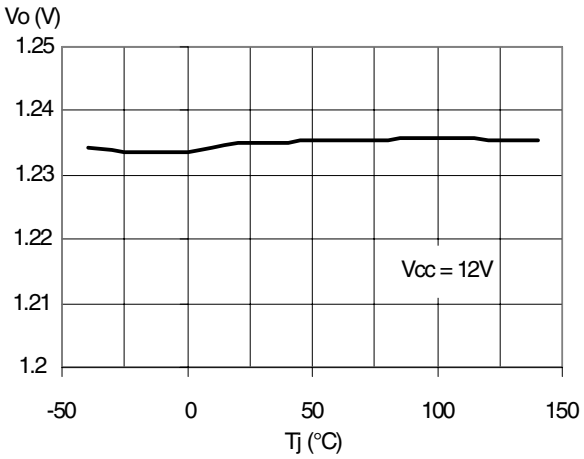


Figure 3. Quiescent Current vs. Junction Temperature

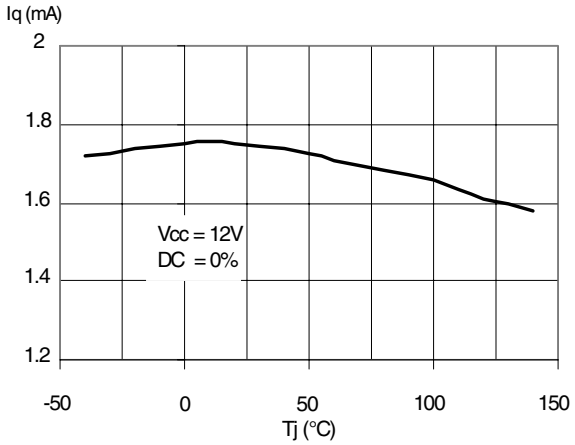


Figure 4. Shutdown Current vs.Junction Temperature

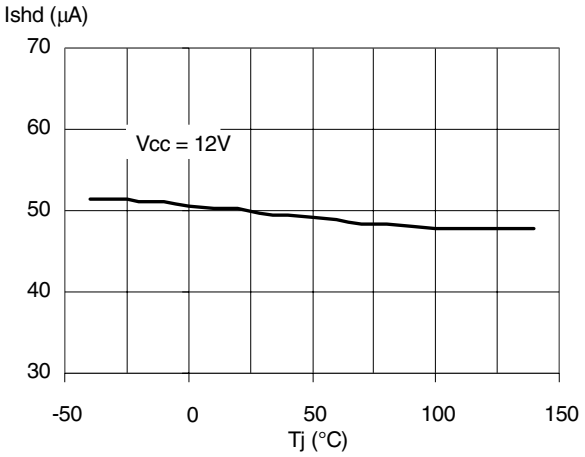
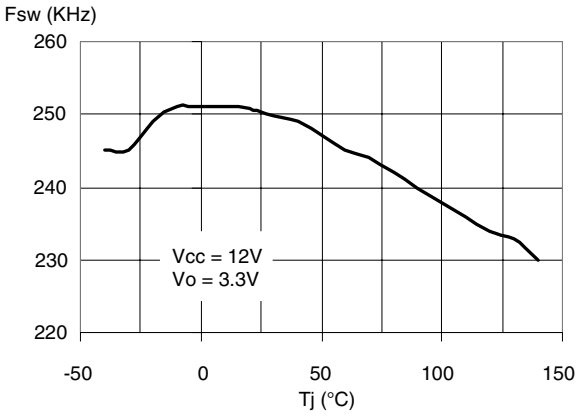


Figure 5. Switching Frequency vs.Junction Temperature



APPLICATION CIRCUIT

In figure 6 is shown the demo board application circuit, where the input supply voltage, V_{cc}, can range from 4.4V to 25V due to the rated voltage of the input capacitor and the output voltage is adjustable from 1.235V to V_{cc}.

Figure 6. Demo board Application Circuit

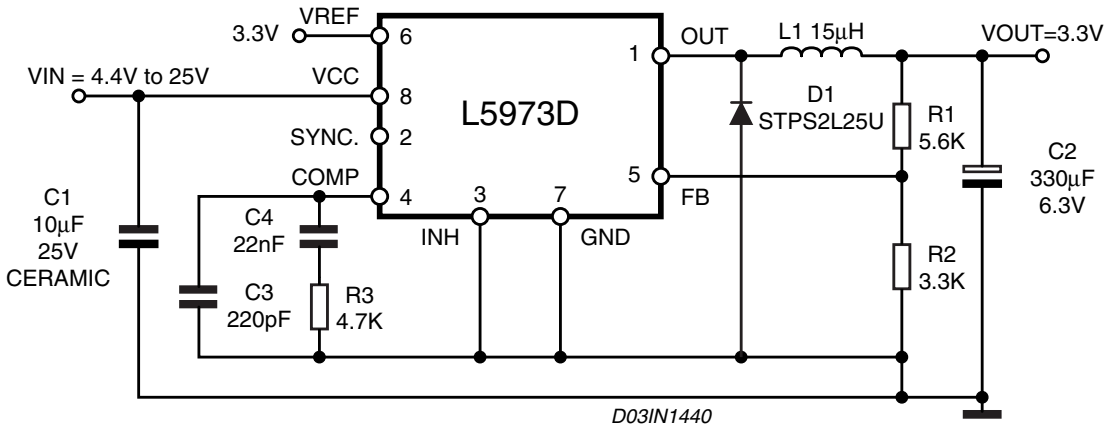


Table 1. Component List

Reference	Part Number	Description	Manufacturer
C1		10µF, 25V	TOKIN
C2	POSCAP 6TPB330M	330µF, 6.3V	Sanyo
C3	C1206C221J5GAC	220pF, 5%, 50V	KEMET
C4	C1206C223K5RAC	22nF, 10%, 50V	KEMET
R1		5.6K, 1%, 0.1W 0603	Neohm
R2		3.3K, 1%, 0.1W 0603	Neohm
R3		4.7K, 1%, 0.1W 0603	Neohm
D1	STPS2L25U	2A, 25V	ST
L1	DO3316P-153	15µH, 3A	COILCRAFT

Figure 7. PCB layout (component side)

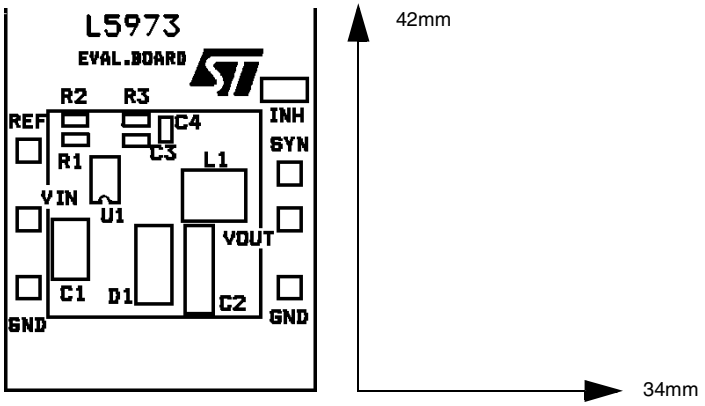


Figure 8. PCB layout (bottom side)

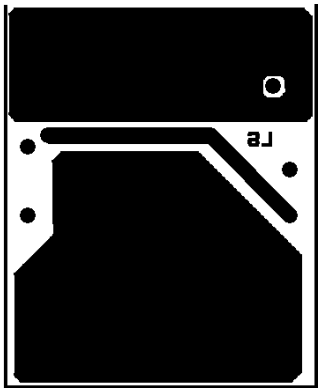
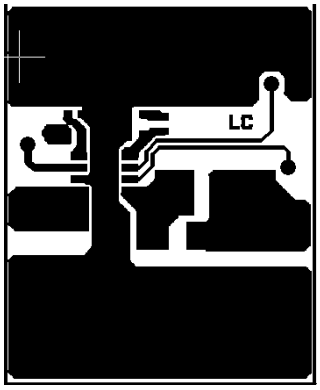


Figure 9. PCB layout (front side)



Below some graphs show the Tj versus output current in different conditions of the input and output voltage and some efficiency measurements.

Figure 10. Junction Temperature vs. Output Current

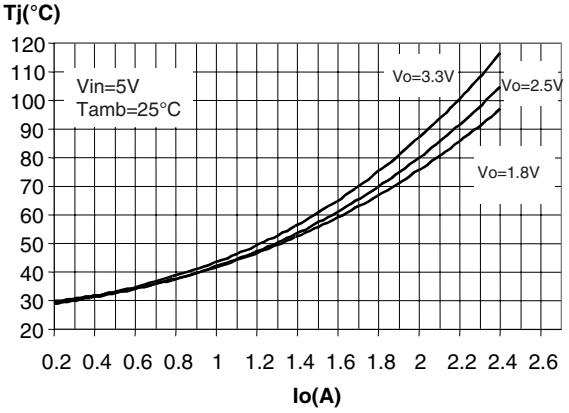


Figure 11. Junction Temperature vs. Output Current

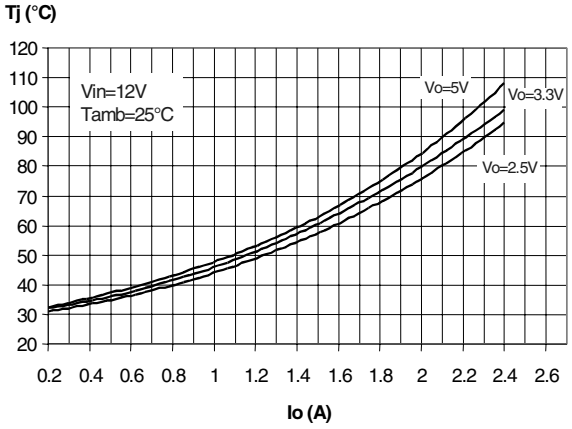


Figure 12. Efficiency vs. Output Current

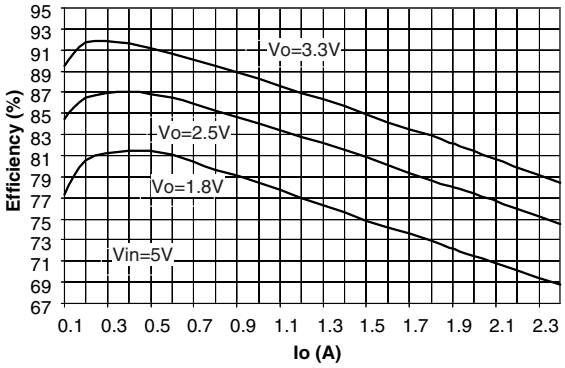
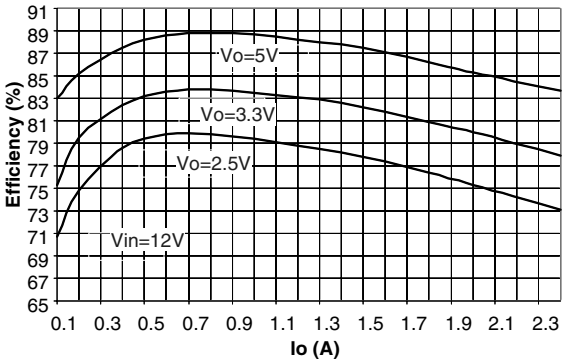


Figure 13. Efficiency vs. Output Current



APPLICATION IDEAS

Figure 14. Positive Buck-Boost regulator

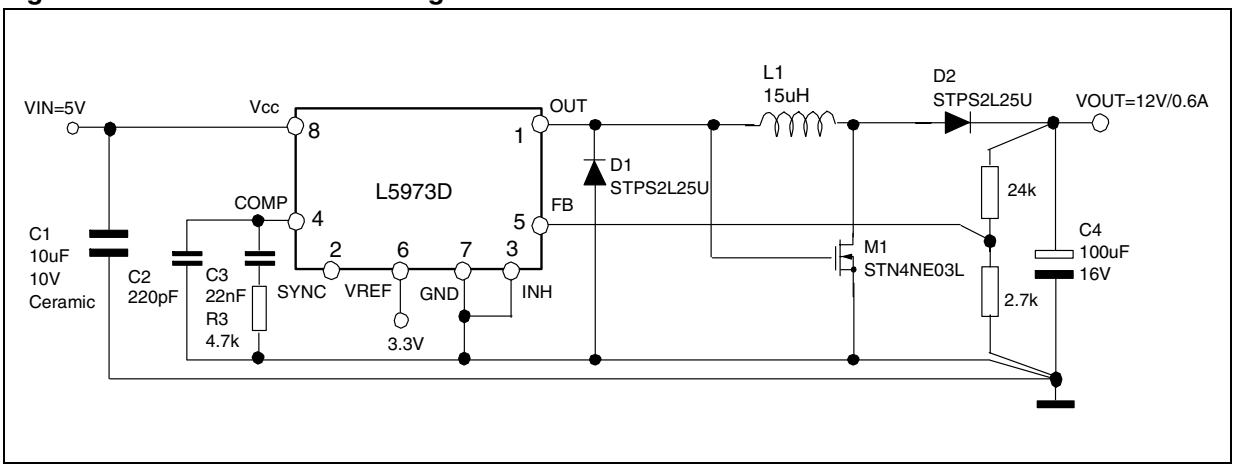


Figure 15. Buck-Boost regulator

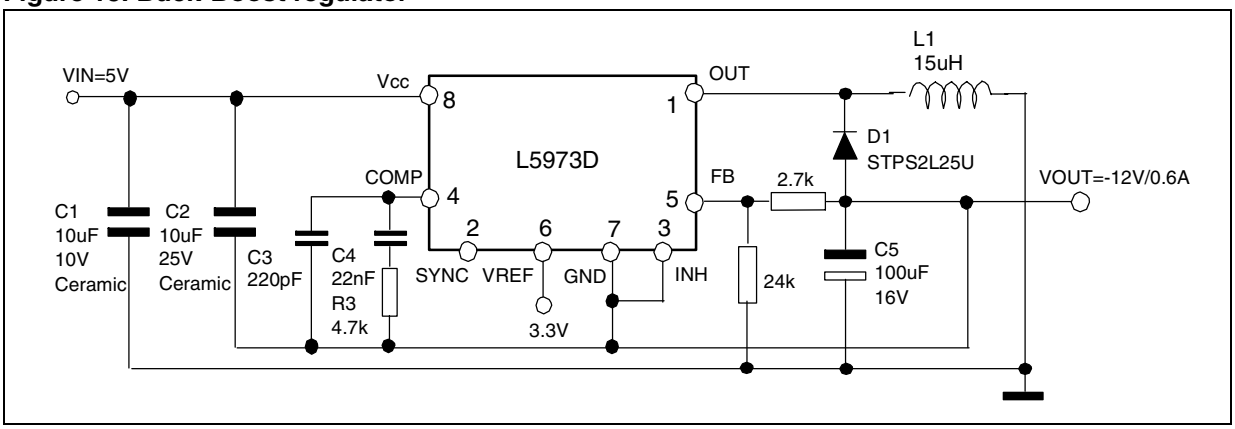


Figure 16. Dual output voltage with auxiliary winding

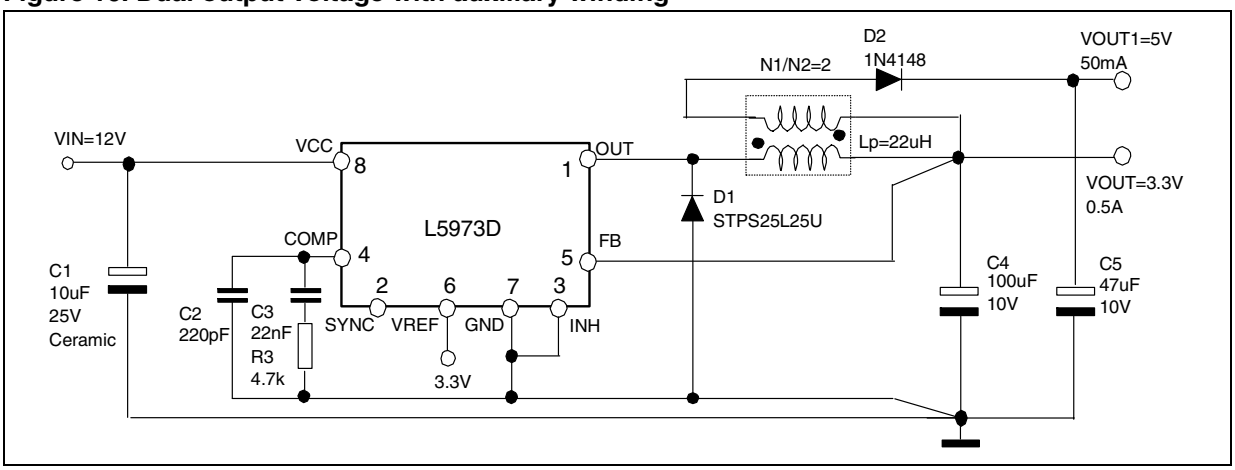
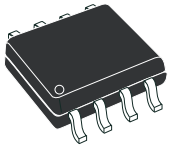


Figure 17. HSOP8 (Exposed Pad) Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.70			0.0669
A1	0.00		0.15		0.00	0.0059
A2	1.25			0.0492		
b	0.31		0.51	0.0122		0.0201
c	0.17		0.25	0.0067		0.0098
D (1)	4.80	4.90	5.00	0.1890	0.1929	0.1969
D1 (3)	ACCORDING TO PAD SIZE					
E	5.80	6.00	6.20	0.2283		0.2441
E1 (2)	3.80	3.90	4.00	0.1496		0.1575
E2 (3)	ACCORDING TO PAD SIZE					
e		1.27				
h	0.25		0.50	0.0098		0.0197
L	0.40		1.27	0.0157		0.0500
k	0		8			0.3150
ccc			0.10			0.0039

Notes: 1. Dimension D does not include mold flash, protusions or gate burrs shall not exeed 0.15mm (both side).
2. Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.
3. The size of exposed pad is variable depending of lead-frame design pad size. End user should verify “D1” and “E2” dimensions for each device application.

OUTLINE AND MECHANICAL DATA



HSOP8 (Exposed Pad)

Exposed Pad:
D1 = 3.1mm
E2 = 2.41mm

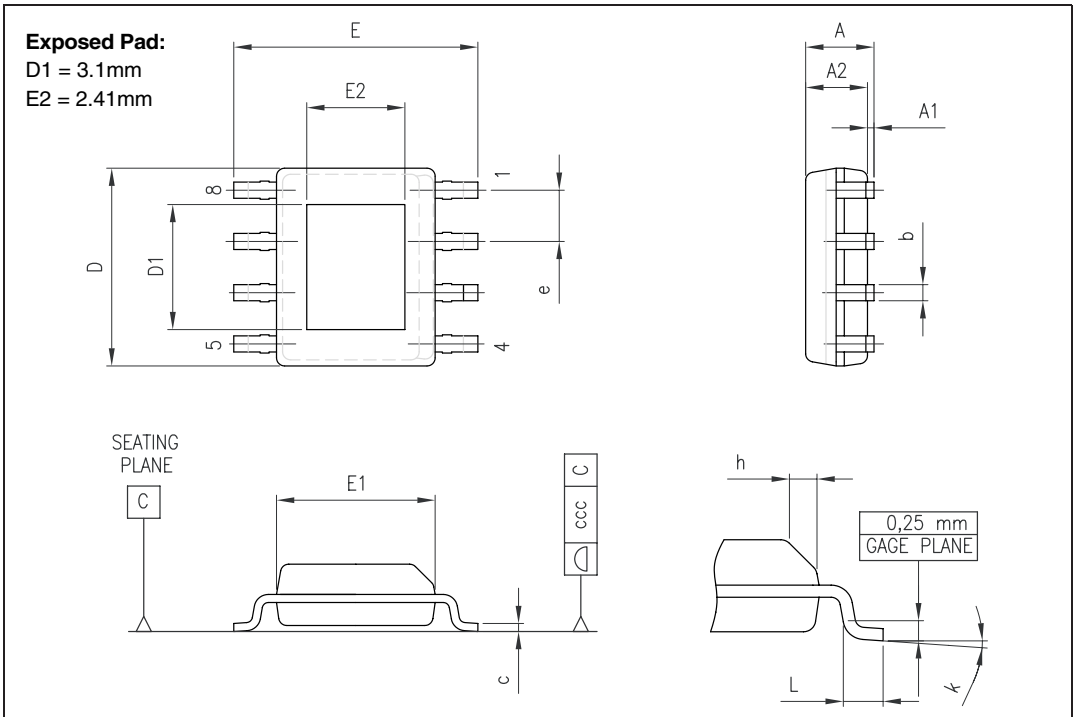


Table 2. Revision History

Date	Revision	Description of Changes
September 2003	9	First issue in EDOCS.
November 2005	10	Updated Package Information Figure 17.